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Fully digital and White Rabbit synchronized Low Level RF System for LIPAc

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***Abstract*— The International Fusion Materials Irradiation Facility (IFMIF) is an international project to study and qualify candidate materials for the construction of a future fusion reactor. One of the objectives of the IFMIF-EVEDA (IFMIF-Engineering Validation and Engineering Design Activity) project is to build a Linear Prototype Accelerator (LIPAc) to validate the final IFMIF accelerator concept. LIPAc, which is currently under construction in Rokkasho (Japan), will generate a 9 MeV deuteron beam of 125 mA current with a 100% of duty cycle. CIEMAT (Spain) is in charge of providing the RF Power System, including the Low-Level Radio Frequency (LLRF) system.**

Most of the developed LLRF systems are not completely digital, as they use analog front-ends for intermediate frequency (IF) conversion before or after digitalization. However, the LIPAc LLRF System is a fully digital system: no analog frequency conversion is performed, the radiofrequency (RF) signals are direct digitally synthesized and sampled by means of high speed DACs (Digital to Analog Converters) and ADCs (Analog to Digital Converters). This is a clear advantage in terms of flexibility, reliability, reconfigurability, cost, and response time, as all signal processing is performed in the digital domain. The other main advantage and novelty is the use of White Rabbit (WR) for timing synchronization and Master Oscillator distribution (distributed RF over WR, WR-DRF). LIPAc LLRF System is the first LLRF based on White Rabbit, and it has been designed and fabricated using the most advanced technology. This paper presents the detailed description of the LIPAc LLRF System, its advantages, performance evaluation, and verification.

***Index Terms*—Accelerator technology, accelerator control systems, accelerator RF systems, Low-level radio frequency, FPGA, digital signal processing.**

I. Introduction

After the migration of the LLRF Systems to In-Phase and Quadrature (I-Q) control in the 90's [1], traditional LLRF designs for accelerators have been based on the use of analog I-Q mod/demodulators for the RF signal generation/ demodulation [2],[3]. The most widely adopted architecture has been the homodyne or zero-IF, where the RF signal is directly down-converted to zero frequency by means of an I-Q demodulator and a local oscillator (LO) of the same frequency. After low-pass filtering, baseband I-Q components can be directly obtained (baseband sampling). Zero-IF architecture has some important limitations, such as DC-offset, 1/f noise, I-Q imbalances, LO leakage, and second-order intermodulation distortion [4]. However, it presents benefits with respect to heterodyne: there is no image frequency (therefore no costly image rejection filters are required), main operations are baseband performed, which leads to higher level of integration, compact size, simplicity, low-power consumption, flexibility, and system reconfigurability [5].

Migration toward digital systems and Software Defined Radio architectures is the trend at the present moment. In the last years, most of the LLRF systems have been upgraded to partially-digital architectures, which combine an analog heterodyne architecture with digital IF synthesis/IF sampling [6]-[9]. Zero-IF architectures have incorporated recent digital signal control and processing technologies, and they are still used in LLRF systems [10], mainly in the RF generation part combined with IF sampling [11]-[18]. Nevertheless, in general terms and in particular for linear accelerators applications, LLRF Systems performance continues to be limited mainly by analog components, especially for high frequency applications, where it is not possible to eliminate analog frequency conversion circuits before or after digitalization, due to current state-of-art on DACs/ADCs.

A first half-digital LLRF prototype was developed by CIEMAT in collaboration with CELLS [19]-[20]. It was based on direct digital demodulation (direct sampling), but for RF signal generation an analog front-end was used for up-conversion from IF to final RF.

The LIPAc LLRF System described in this paper is a novel, fully digital, and WR synchronized LLRF System, where both RF signal generation and demodulation are fully performed in the digital domain. IFMIF demands very challenging requirements for the LLRF and RF systems, especially regarding flexibility, synchronization, RF field detection precision, signal stability, and RAMI (Reliability, Availability, Maintainability and Inspectability) [21]. Some main specifications for the LIPAc LLRF System are compiled in Table 1. Note that extra flexibility is required not only in the RF operational regime (continuous and pulsed), but also in the

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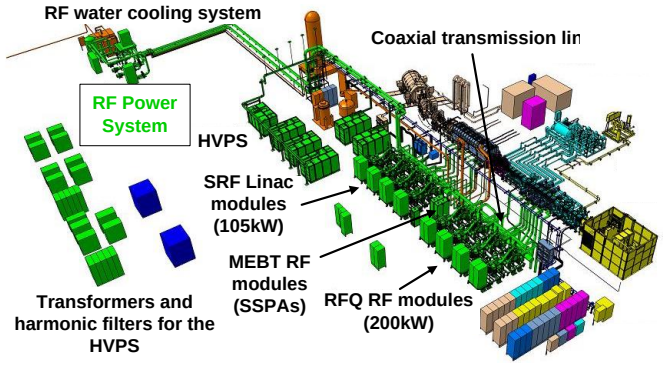


Fig. 1. 3D schematic of the LIPAc RF Power System.

LLRF output frequency, which has to be dynamically shifted ±300kHz. In order to fill the cavities when they are not tuned to the nominal frequency, and the cavity tuning systems are too slow to reach tuning condition, the LLRF dynamically changes its frequency to follow the cavity resonance frequency. This is required in two situations: during the start-up of the RFQ cavity, where the power increases up to 200 kW, and the power dissipation produces a temperature increment that modifies the cavity resonance frequency; and for beam loading compensation in pulse mode operation, in order to pre-fill the cavities before the beam arrival (the tuning systems keeps the cavities tuned to the nominal frequency when there is beam and therefore they are detuned before the beam arrival). Another challenging specification is the synchronization of several RF chains in order to operate as a unique chain, coincident in time and with the same amplitude and phase. Consequently, many efforts have been focused on the development of a robust, innovative, and cutting-edge LLRF System, capable to fulfill very demanding specifications. A complete digital and WR-compliant design multiplies the advantages and possibilities, as it will be explained in sections III and IV, where the main characteristics and innovations of the LIPAc LLRF System will be presented. LLRF is part of the LIPAc RF Power System, which will be briefly described in Section II. The measured performance and validation test of the LLRF system will be presented in Section IV.

TABLE 1 LIPAC LLRF SYSTEM MAIN REQUIREMENTS

Parameter	Value/description
Cavity types	1 RF Quadrupole (RFQ) 2 re-buncher cavities 8 superconducting half-wave resonators
Nominal Frequency	175 MHz
Frequency shift	±300 kHz, for real-time cavity resonance frequency tracking
Stability (closed loop)	±1% in amplitude ±1º in phase
RF operational regime	CW and pulsed mode
Emergency RF stop	< 10 µs (at the cavity input)
Cavity tuning	1º resolution
RF chains balance and syncronization	Amplitude/phase balance and time synchronization to operate as a unique RF chain
RAMI	98.2% availability

II. LIPAc RF Power System

The LIPAc RF Power System [21]-[25] consists of 18 RF chains operating at 175 MHz, 12 400 kW high voltage power supplies (HVPS), 18 coaxial transmission lines to reach the accelerator cavities, and the water cooling system primary circuit. The 3D view of the LIPAc accelerator is presented in Fig. 1, where all RF System components are represented in green color.

The 18 RF chains are structured in 9 RF modules (two RF chains form one RF module), and are distributed as follows:

- Eight 200 kW RF chains (four 2x200kW RF modules) for the RFQ.
- Two 16 kW RF chains (one 2x16kW RF module) for the two re-buncher cavities of the Medium Energy Beam Transport (MEBT).
- Eight 105 kW RF chains (four 2x105kW RF modules) for the eight superconducting half-wave resonators of the SRF Linac.

For standardization and scale economy reasons, the 200kW and 105kW RF chains share the same topology and main components, and they only differ in the circulator. They consist of three amplification stages: a first solid-state pre-driver, and two tetrodes for driver and final amplifiers. Two RF chains compose one RF module, as they share some common elements such as the mechanical structure for the circulators and tetrodes, the water and air cooling circuits, the LLRF unit, the PLC (Programmable Logic Controller), the arc detector system, the protection system, etc. Tetrode RF modules for RFQ and SRF Linac have been developed by CIEMAT and its partner company INDRA, under CIEMAT conceptual design. The 3D-mock-up of the tetrode-based RF module is represented in Fig. 2.

The 2x16 kW RF module for MEBT is based on solid state (SS) technology, and can be seen in Fig. 3. Each RF chain contains two SS amplification stages: a first predriver amplifier, and a final amplifier, which is formed by the combination of 10 SS Power Amplifiers (PA). Both RF chains share some common elements (LLRF, arc detector, PLC, etc). The detailed design and fabrication of the SS RF module are made by the Spanish company Broad Telecom (BTESA) under CIEMAT conceptual design.

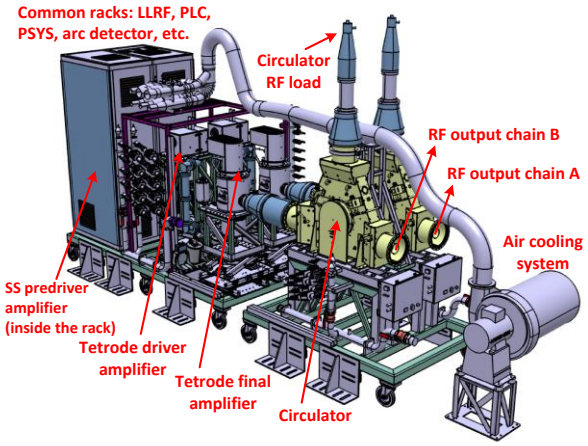


Fig. 2. Tetrode-based RF module.

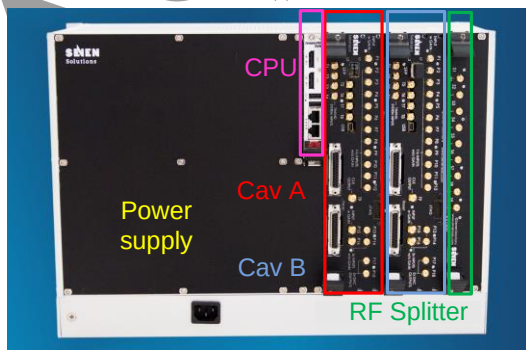
Fig. 3. Solid-state 2x16kW RF module.

The 400 kW HVPSs (up to 13 kV and 45 A) for the tetrode-based amplification changes are designed and manufactured by JEMA Energy (San Sebastián, Spain).

III. LIPAc LLRF System Description

The LIPAc LLRF system consists of nine LLRF units. A photograph of one LLRF unit is shown in Fig. 4. It can be also seen integrated in one rack of the solid-state 2x16kW RF module in Fig. 3.

(a)



(b)

Fig. 4. LLRF unit: (a) front view, (b) rear view.

Each LLRF unit is designed to control two RF cavities. Fig. 5 shows the LLRF block diagram with the different elements and connections needed to control one RF cavity. The main implemented functionalities are described below:

- Cavity field amplitude and phase control (feedback loop).
- Signal diagnostics and data remote access.
- Cavity tuning: manual and automatic.
- Conditioning: manual and automatic.
- Fast interlock management: arcs, reflected power, max. forward power, multipacting, vacuum, etc.
- Continuous wave (CW) and pulse operation modes.
- Frequency modulation: manual and automatic.
- Feed-forward loop: cavity pre-filling, beam loading compensation.
- Timing synchronization and Master Oscillator distribution using White Rabbit (WR-DRF).
- Fast data logger for post mortem analysis.
- Automatic start-up.
- Master-slave feedback loop (specific for RFQ): synchronization of the eight RFQ RF chains to operate as a unique chain, one as master and seven as slaves.
- Temperature dependence compensation.

A. *Hardware description*

The LLRF unit is a compact and fully integrated system. It is based on a modular design, as shown in Fig. 4, where the different boards can be easily extracted and substituted in order to improve the availability. Each LLRF unit is composed of:

- One Compact-PCIe Serial (cPCI-S) rack enclosure.
- One cPCI-S backplane.
- One 200W Power Supply.
- One cPCI-S CPU (G20–3U CompactPCI® Serial Intel® Core™ i7 CPU Board).
- Two 6U integrated-board modules, composed of several boards arranged in a sandwich distribution. Each integrated-board module controls one cavity and performs all the described functionalities. It is described in more detail in Section IV.
- One 6U 1:8 RF splitter (specific for RF Quadrupole).

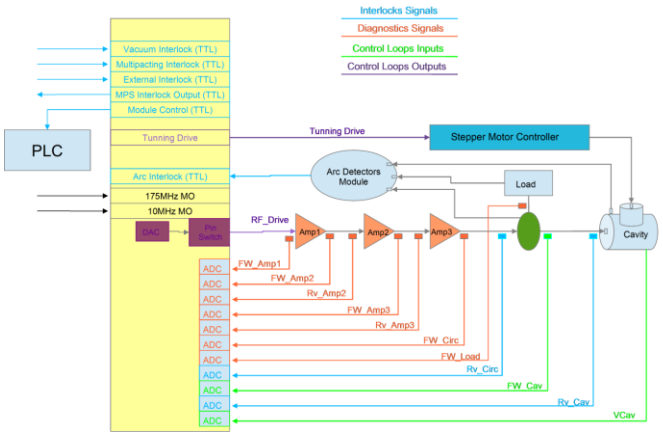


Fig. 5. LLRF Block diagram for one cavity control.

B. *Software architecture*

LIPAc LLRF control system is based on the Experimental Physics and Industrial Control System (EPICS). EPICS is a software environment used to develop and implement distributed control systems to operate devices such as particle accelerators, telescopes, and other large experiments. EPICS control systems work with a Client/Server architecture. Fig. 6 shows a schematic of the LLRF software architecture.

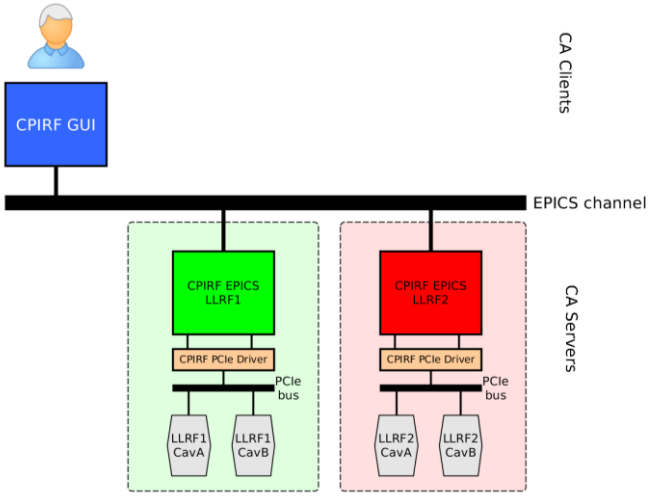


Fig. 6. LLRF Software Architecture.

C. *User interface*

The graphical user interface (GUI) has been developed using CSS BOY (see Fig. 8). The design takes into account the previous experience of the different European Institutes involved in the LIPAc project, which have elaborated some recommendations and standards that follow basic rules such as simplicity, efficiency, intuitive structure, user friendly environment, etc.

D. *White Rabbit*

The generation and distribution of the timing reference signals is crucial for preserving the synchronization into an accelerator facility. The LIPAc Timing System, which is developed by QST (Japan), provides the 10 MHz Master Clock (MC) signal to the different accelerator systems, including the RF System. CIEMAT is in charge of distributing the MC to the overall RF System, keeping signal integrity and synchronization among the 18 RF chains. Furthermore, CIEMAT is responsible of the generation and distribution of the 175 MHz Master Oscillator (MO) reference signal. The MO has to be a very stable signal locked to the MC, in order to act as timing reference for the accelerator sub-systems. MO is required at each LLRF and also at some external systems like the Beam Position Monitors (BPMs).

The classical solution consists of generating both MC and MO signals by means of phase-locked high quality signal generators, and split these signals using well-balanced analog distribution networks with conventional coaxial cables. This solution is problematic because it is very sensitive to environmental conditions, temperature fluctuations, humidity changes, material aging, losses variations, calibrations exactness, etc. Consequently, with this configuration it is difficult in practice to achieve a perfect balance among all branches and therefore high-precision synchronization. Another drawback is that a high isolation is required in the coaxial cables, since they cross very emissive environments in an accelerator facility. Alternatively, CIEMAT and Seven Solutions have developed a timing distribution and synchronization system based on WR for both MC and MO reference signals, whose scheme is shown in Fig. 7. It consists of one Master WR Switch and one Slave WR Switch, which communicates with the nine WR-compliant LLRF units by optical fibers. Optical technology has clear benefits for synchronization reference distribution for large facilities, as it provides less signal attenuation and larger bandwidths, and alleviates the above mentioned problems of conventional coaxial cables. For not-compliant WR devices, such as the BPMs in LIPAc, the WR synchronization system includes a WR Clock Box, which is connected by optical fiber to the WR node, and provides a stable MO (phase noise<1ps) through coaxial cable.

WR is a fully deterministic Ethernet-based network that provides ultra-accurate synchronization and gigabit data transfer capability. It was born in CERN for time and frequency dissemination, and it has been conceived to fulfill the following goals:

- Time precision: WR technology provides a common clock for physical layer in the entire network, allowing synchronization at sub-nanosecond level with picoseconds precision.
- Scalability: the WR network is designed to be highly scalable to support thousands of nodes. It also intends to be as modular as possible, and compatible with non-WR devices.
- Distance range: taking into account the size and ranges of the majority industrial and scientific facilities, the WR network specifications have been designed to support distances up to several tens of kilometers between nodes.

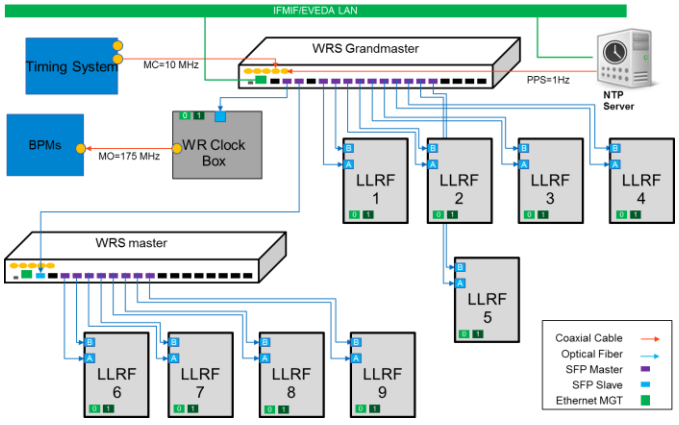


Fig. 7. Timing reference distribution using White Rabbit.

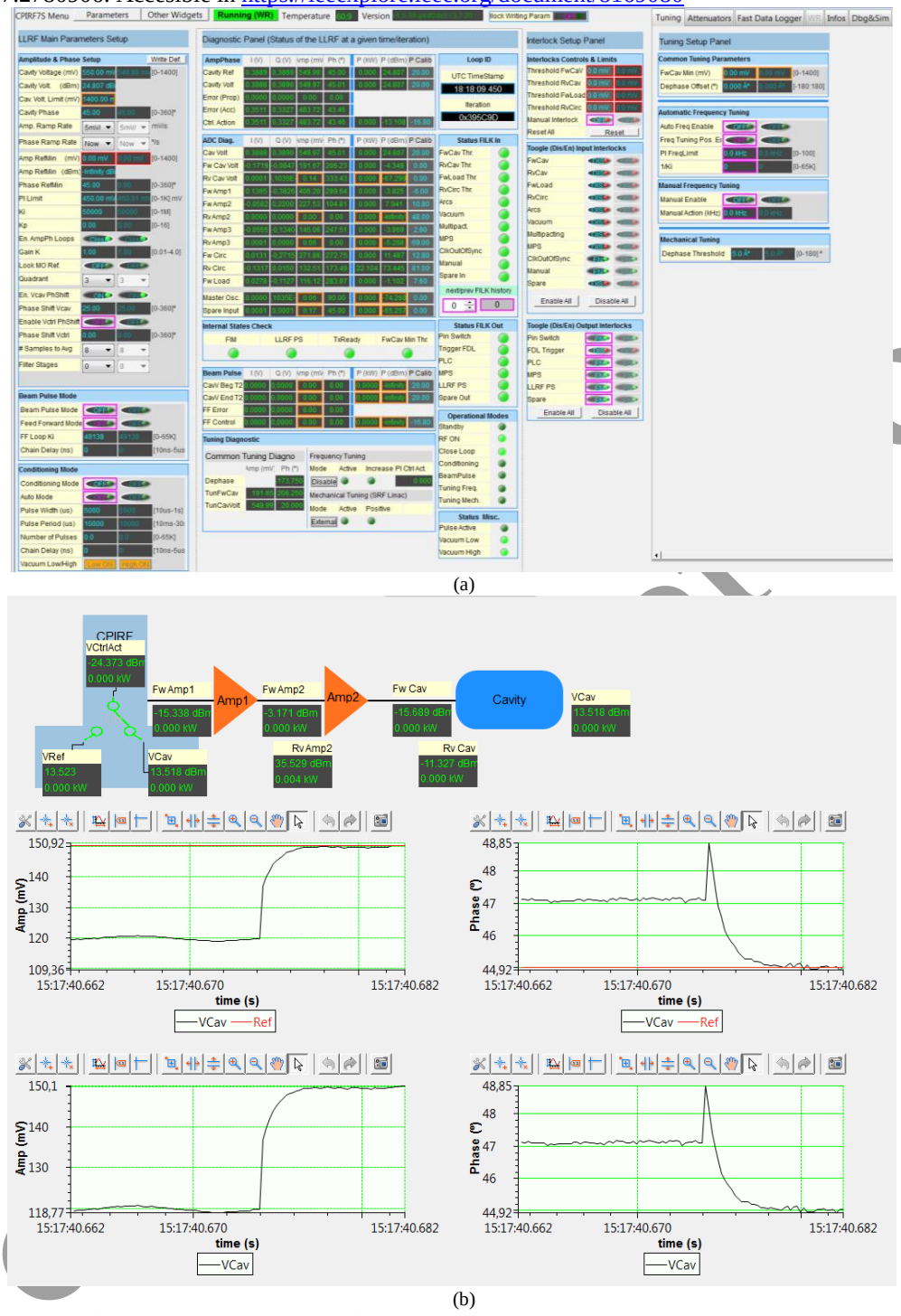


Fig. 8. LLRF Graphical User Interface (a) main view (b) example of diagnostic.

IV. Direct Digital RF Synthesis and Demodulation

The LIPAc LLRF is a fully digital system, where both RF synthesis and demodulation are completely performed in the digital domain. The system concept is shown in Fig. 9. Focusing on the RF demodulation part, undersampling technique, also known as direct bandpass sampling, is used for the 175MHz signal acquisition and the in-phase (I) and quadrature (Q) components detection (sampling frequency f_s=100 MHz). Regarding the RF generation side, two 175MHz signals are directly generated by means of fast DACs, working at f_s=700 MHz. Let us represent the RF signal in terms of its I/Q components as follows:

$$v(t) = I \cdot cos(2\pi f_c t) - Q \cdot sin(2\pi f_c t) \quad (1)$$

where f_c is the nominal 175 MHz frequency, and t is the time. The digitalized signal results in:

$$v\left(\frac{n}{f_s}\right) = I \cdot cos\left(2\pi f_c \cdot \frac{n}{f_s}\right) - Q \cdot sin\left(2\pi f_c \cdot \frac{n}{f_s}\right) \quad (2)$$

being n=0,1,2,... Notice that the factor f_c/f_s =1.75 has been

selected for the demodulation, which substituted in (2) results in the sequence: I, Q, -I, -Q, I, Q, ... For the RF generation, the

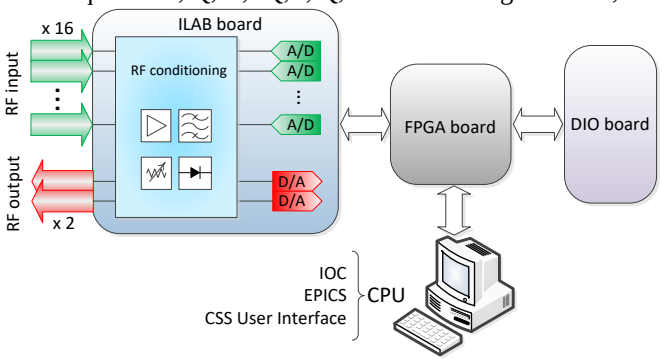


Fig. 9. System schematic description: direct RF signal synthesis/acquisition.

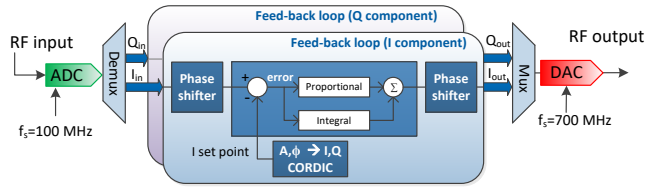


Fig. 10. Feed-back loop block diagram.

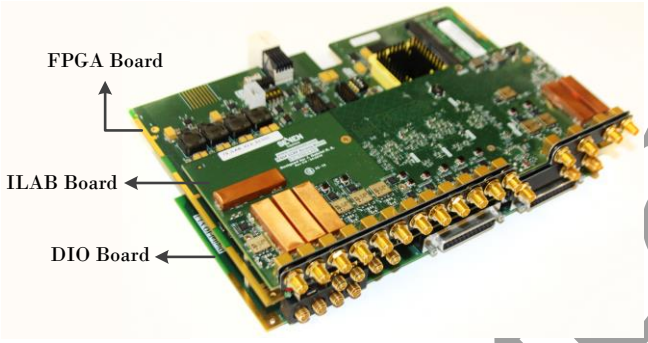


Fig. 11. Photograph of the integrated-board module.

relation f_c/f_s is 1/4, which leads to: I, -Q, -I, Q, I, -Q, … Note that the I-Q components can be easily obtained by demultiplexing/multiplexing the samples, and applying a phase inversion. Using such multiples of 175MHz is very advantageous, as the FPGA can work directly with I/Q components, which simplifies the signal processing and reduces the FPGA computational load.

The cavity field feedback loop is a Proportional-Integral (PI) loop that applies directly to I/Q components, whose block diagram is presented in Fig. 10. Amplitude and phase values can be easily obtained from IQ components as follows:

$$A = \sqrt{I^2 + Q^2} \quad (3)$$

$$\phi = atan\left(\frac{Q}{I}\right) \quad (4)$$

These operations are carried out in the FPGA by means of the CORDIC algorithm.

Each board shown in Fig. 9 is arranged in a sandwich distribution forming an integrated-board module (see Fig. 11), composed of:

1) ILAB board: it integrates a RF conditioning front-end and fast ADCs/DACs. The RF front-end is a signal adaptation stage, without analog frequency conversion, which contains:
   - 16 SMA input channels: based on filters, and SW controllable attenuators. There are two channels with additional amplification, dedicated for low power RF signals.
   - 2 SMA output channels: based on filters, SW controllable attenuators, amplifiers, and absorptive pin diode switches for fast RF stop.

   Connected to these RF conditioning paths, there are 2 DACs (1.25 Gsps, 16 bits, -60 to +14 dBm dynamic range), and 16 ADCs (125 Msps, 14 bits, -40 to +17 dBm dynamic range). ILAB board is connected to the FGPA board by a double FMC (FPGA Mezzanine Card).
2) FPGA board: based on Xilinx Virtex-6 (LX240T) FPGA and a 2GB DDR DIMM (Double Data Rate, Dual In-line Memory Module). Its block diagram is shown in Fig. 12. It includes the Clock Generation block, which is responsible of providing the different clocks to the system, using a high-performance VCXO (Voltage-Controlled Crystal Oscillator), and a Phase-Locked Loop (PLL).
3) Digital Input/Output (DIO) board: digital I/O signals (DB-25 connectors) for interlocks, cavity tuning signals, and other communications with external subsystems. Timing System trigger/gate signals (SMA) for beam synchronization.

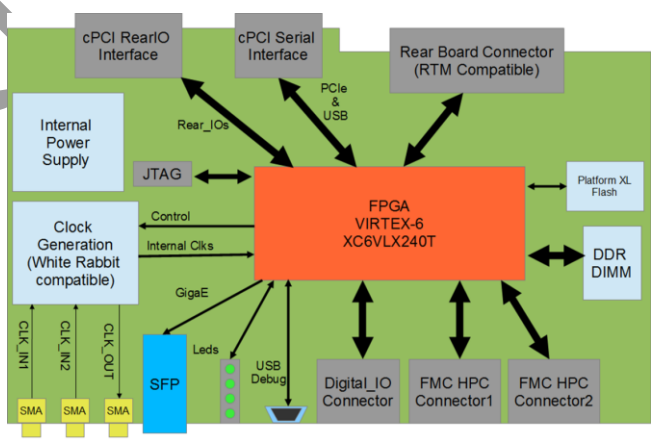


Fig. 12. Block diagram of the FPGA board.

V. LLRF PERFORMANCE AND VALIDATION

All the LLRF functionalities described in Section III have been satisfactorily proved and validated. Table 2 summarizes the basic main performance of LLRF system in stand-alone mode (not connected to the RF chains). The system can operate in CW and pulsed regime (min. 10 µs pulse width). The nominal output frequency is 175 MHz, which can be dynamically shifted ±300 kHz to compensate cavity detuning, in manual or automatic mode (cavity resonance frequency tracking). It is observed a good quality of the LLRF 175 MHz output signal, which is locked to the MO reference distributed by WR: <-60 dBc harmonics rejection, and <-65 dBc spurious rejection. The output power can be selected between -60 dBm and 14 dBm (74 dB dynamic range). A very good RF signal

stability, which is a main parameter for LLRF systems, has been achieved when working in stand-alone closed feedback loop (direct wire connection between LLRF RF output and input): 0.08º of rms phase variation (100 Hz-1 MHz), and 0.0051% rms variation in voltage amplitude. Another important parameter is the emergency RF stop, that is, the time between an alarm is detected and the RF output signal is switched off. The measured emergency RF stop time is only 800 ns in stand-alone mode.

TABLE 2 LLRF BASIC PERFORMANCE (STAND-ALONE)

Parameter	Measured value
Operational regime	CW/pulsed
Nominal frequency	175 MHz
Frequency shift	± (0.1 – 300) kHz
Output power	-60 dBm to +14 dBm
Amplitude stability	0.0051% rms
Phase stability	0.08º rms
Harmonics level	<-60 dBc
Spurious level	<-65 dBc
Emergency RF stop	~ 800 ns

The LLRF has been integrated and validated with the LIPAc high power RF modules in Madrid (Spain), at INDRA and BTESA facilities. Currently, the RF modules for RFQ and MEBT are installed in Rokkasho (Japan), where they are being commissioned [26]. Table 3 compares the LIPAc RF Power System requirements with the measured performance for one 200 kW tetrode-based RF chain, while Table 4 presents the results for one 16 kW solid-state RF chain. As it can be seen, all parameters fulfill the specified requirements. Similar results are obtained in the rest of RF chains.

TABLE 3 2ND RFQ 2X200 KW RF MODULE: CHAIN A PERFORMANCE

Parameter	Acceptance Criteria	Measured value
Frequency	175 MHz	175 MHz
Bandwidth	±250 kHz @ -1dB	-0.18dB @ 250 kHz
Phase stability (closed loop)	±1º	0.0945º rms
Amplitude stability (closed loop)	±1%	±0.26 peak (*)
Output RF power	200 kW CW	220 kW CW > 20 h
Full reflected power	10 µs	Full reflection (200kW): 100 ms
Maintained reflected power	20 kW, 2h	40kW > 2h
Operating mode	CW	CW. Also validated in pulsed mode (from 2 µs pulse witdh to CW)
Emergency RF stop	< 10 µs	1.98 µs
Harmonics Level	< -30 dBc	-51.17 dBc
Spurious Level	< -30 dBc	<-75 dBc

(*) Peak error

Focusing on the parameters that are more related to LLRF performance, it is important to pay attention to the amplitude and phase signal stability results. RF signal stability is crucial for accelerators performance, and very good results have been achieved. A 0.0945º rms phase error is obtained for the 200kW RF chain, and 0.13º rms for the SS 16 kW chain. The phase error has been quantified in terms of the phase jitter (ºrms), which can be obtained from the phase noise

TABLE 4 SOLID STATE 2X16KW RF MODULE: CHAIN A PERFORMANCE

Parameter	Acceptance Criteria	Measured value
Frequency	175 MHz	175 MHz
Bandwidth	±250 kHz @ -1dB	-0.04dB @ 250 kHz
Phase stability (closed loop)	±1º	0.13º rms
Amplitude stability (closed loop)	±1%	±0.16% peak (*)
Output RF power	16 kW CW	16 kW CW > 12 h Max. 20 kW
Full reflected power	10 µs	Full reflection (16kW): 120 ms
Maintained reflected power	4 kW, 2h	4.8kW > 2h
Operating mode	CW	CW. Also validated in pulsed mode (from 2 µs pulse witdh to CW)
Emergency RF stop	< 10 µs	1.08 µs
Harmonics Level	< -30 dBc	-42.62 dBc
Spurious Level	< -30 dBc	-70.67 dBc

(*) Peak error

TABLE 5 PHASE NOISE MEASUREMENTS (SS 16 KW CHAIN)

Freq. offset	Phase noise (dBc/Hz)
100 Hz	-92
1 kHz	-105
10 kHz	-109
100 kHz	-109
1 MHz	-127
Phase jitter (ºrms)	0.13

TABLE 6 AMPLITUDE STATISTICAL DISPERSION PARAMETERS

Parameter	200 kW RF chain	16 kW SS chain
Observation time	2 hours	2 hours
Num. of samples	7753	1463
Range (Max - Min)	0.34%	0.28%
Standard deviation (σ)	0.087%	0.055%
Peak error (±3σ)	±0.26%	±0.16%

measurements [27]. For the 200 kW chain, the measurement has been automatically performed using the R&S®FSU3 Spectrum Analyzer (option R&S®FS-K40). For the SS 16 kW chain, the phase noise measurements compiled in Table 5 have been used. In regard to the amplitude stability test, the RF chains were kept at maximum power during two hours, meanwhile the amplitude of the RF signal was measured by a power meter (Agilent N1914A power meter and high precision N8482A sensors, no averaging applied), and the data were transferred to a Personal Computer. The measured voltage amplitude with respect to time is plotted in Fig. 13. Statistical results for voltage amplitude variation, calculated from the measured data, are shown Table 6. Peak voltage amplitude error has been calculated considering the three-sigma rule: 99.7% of cases are taken to lie within ± three standard

deviations (±3σ) from the mean, which can be empirically treated as near certainty. Consequently, the results are ±0.26% for the 200kW RF chain, and ±0.16% in the 16 kW SS chain. Note that this convention is more pessimistic than the range given by the measured maximum and minimum values. In any case, these figures are quite smaller than the requirement of ±1%.

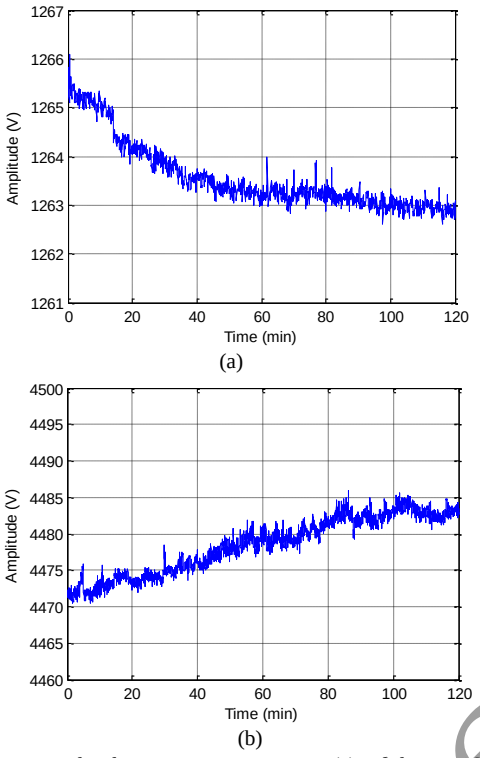


Fig. 13. Voltage amplitude variation versus time: (a) solid state 16 kW RF chain; b) tetrode-based 200 kW RF chain.

Another important parameter for accelerators is the emergency RF stop. In these measurements it is considered the time between an alarm is detected in the LLRF, and the RF at the output of the RF chain is switched off (it includes RF chain propagation delay). Note that LIPAc requirement is <10 µs, and the measured emergency RF stop is 1.98 µs and 1.08 µs for the 200kW and 16kW chains, respectively (see Fig. 14 and Fig. 15).

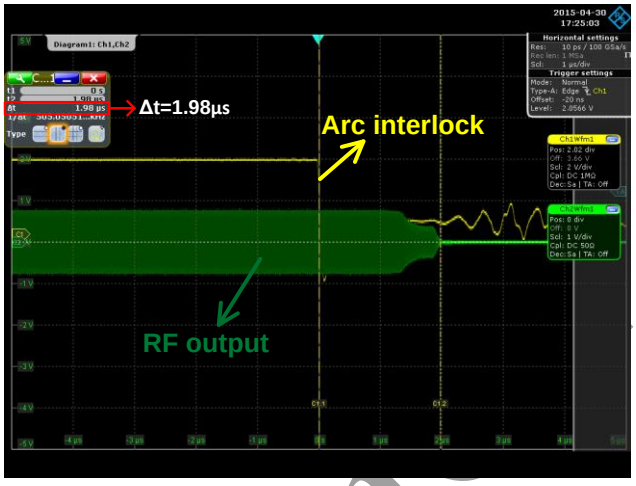


Fig. 14. Emergency RF stop: tetrode-based 200kW RF chain.

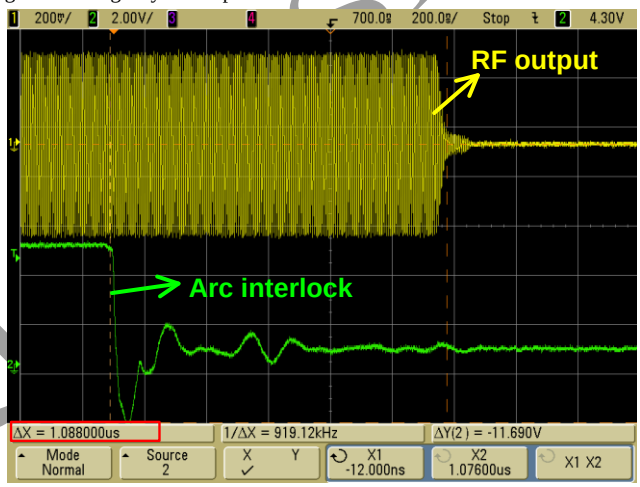


Fig. 15. Emergency RF stop: solid state 16kW RF chain.

The LLRF can operate in CW and pulse modes. Some examples of the pulse mode operation are shown in Fig. 16 and Fig. 17.

Last but not least, the RF signal quality at the output of the RF chains is good, as it can be seen from the harmonics and spurious rejection measurements in Table 3 and Table 4.

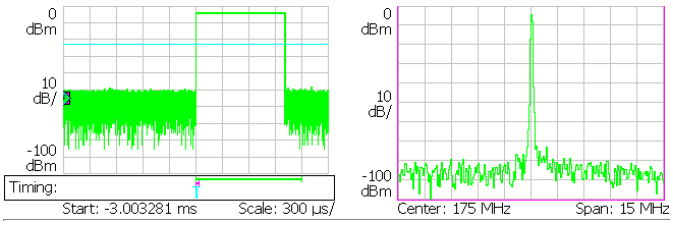


Fig. 16. Pulse mode operation example: 1ms width, 100ms period (solid state 16kW RF chain).

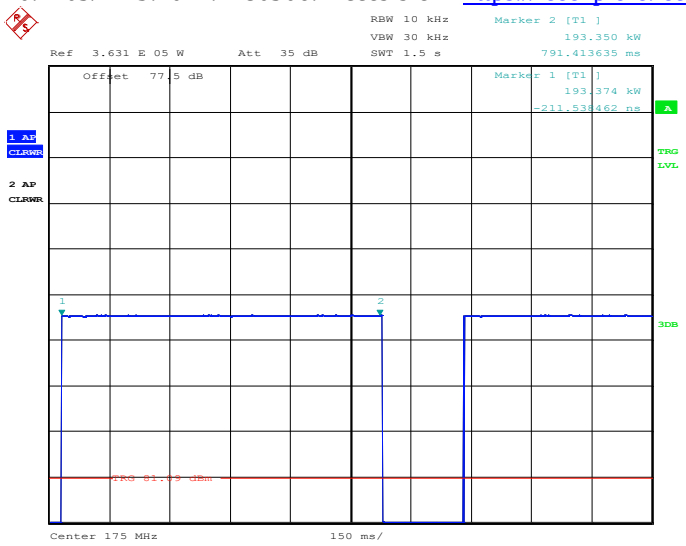


Fig. 17. Pulse mode operation example: 800ms width, 1s period (tetrode-based 200kW RF chain).

VI. Conclusion

The LLRF system for the IFMIF-EVEDA project has been developed and integrated into the LIPAc RF Power System. It has been validated operating with high-power RF chains, exceeding its design specifications. The main advantages and novelties of the LLRF system are presented below:

- Fully digital LLRF: Direct digital synthesis and direct digital sampling (high speed DACs and ADCs). No external front-ends are used for frequency conversion.
- Timing and synchronization based on White Rabbit (CERN). Sub-nanosecond synchronization.
- WR Master Oscillator distribution (WR-DRF).
- Modular design with all functionalities integrated in the same unit.
- Flexible, reconfigurable, and customizable system.
- Fully digital signal processing. Flexible nominal frequency without hardware modifications.
- EPICS ready technology.
- Use of advanced FPGA technology (Xilinx Virtex-6).
- Both MicroTCA and cPCI platforms available.
- Configurable Analog Input module to receive different input signal levels.

All this characteristics traduce in a very flexible and reconfigurable system, where many improvements and modifications can be performed without HW changes, just via firmware: new functionalities, improved and faster control loops, operation frequency migration, fast and efficient frequency modulation, etc. It is worth to mention that the maximum operating frequency in a digital approach is restricted by the performance of state-of-art DAC/ACS, being the main limiting factors the sampling frequency, the resolution, and the jitter.

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